09548826 CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returne

From A Search of 09548826 on February 20, 2004

7 714/718 (4 OR, 3 XR)
Class 714: ERROR DETECTION/CORRECTION AND FAULT
DETECTION/RECOVERY

714/699 PULSE OR DATA ERROR HANDLING

714/718 .Memory testing

6 324/755 (1 OR, 5 XR)

Class 324: ELECTRICITY: MEASURING AND TESTING

324/500 FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC COMPONENTS

324/537 .Of individual circuit component or element

324/754 ..With probe elements

324/755 ...Internal of or on support for device under

test (DUT)

6 324/765 (3 OR, 3 XR)

Class 324: ELECTRICITY: MEASURING AND TESTING

324/500 FAULT DETECTING IN ELECTRIC CIRCUITS AND OF

ELECTRIC COMPONENTS

324/537 .Of individual circuit component or element

324/765 .. Test of semiconductor device

6 365/201 (4 OR, 2 XR)

Class 365: STATIC INFORMATION STORAGE AND RETRIEVAL

365/189.01 READ/WRITE CIRCUIT

365/201 .Testing

4 257/203 (1 OR, 3 XR)

Class 257: ACTIVE SOLID-STATE DEVICES

257/202 GATE ARRAYS

257/203 .With particular chip input/output means

4 257/48 (3 OR, 1 XR)

Class 257: ACTIVE SOLID-STATE DEVICES 257/48 TEST OR CALIBRATION STRUCTURE

4 257/723 (0 OR, 4 XR)

Class 257: ACTIVE SOLID-STATE DEVICES

257/688 .With large area flexible electrodes in press

contact with opposite sides of active semi

conductor chip

and surrounded by an insulating element, e

.g., ring

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257/723 .For plural devices

4 365/233 (0 OR, 4 XR)

Class 365: STATIC INFORMATION STORAGE AND RETRIEVAL

365/230.01 ADDRESSING

365/233 .Sync/clocking

3 257/E21.525 (0 OR, 3 XR)

Class 257: ACTIVE SOLID-STATE DEVICES

257/E21.515Involving use of mechanical auxiliary par

t

without use of alloying or soldering pro

cess, e.g.,

pressure contacts (EPO)

257/E21.521 .Testing or measuring during manufacture or treatment or reliability measurement, i.e.

, testing of

parts followed by no processing which modi

fies parts as

such (EPO)

257/E21.525 ..Procedures, i.e., sequence of activities consisting of plurality of measurement and correction,

marking or sorting steps (EPO)

3 257/E23.171 (0 OR, 3 XR)

Class 257: ACTIVE SOLID-STATE DEVICES

257/E23.139 ...Liquid at normal operating temperature of device (EPO)

257/E23.141 .Arrangements for conducting electric current within device in operation from one compo

nent to another, interconnections, e.g., wires, lead frame

s (EPO)

257/E23.169 ..Interconnection structure between plurality of semiconductor chips being formed on or

in insulating

substrates (EPO)

257/E23.171 ...Adaptable interconnections, e.g., for engineering changes (EPO)

3 257/E25.023 (0 OR, 3 XR)

Class 257: ACTIVE SOLID-STATE DEVICES

257/E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF

INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID-

STATE DEVICES (EPO)

					09548826 CLSTITLES
			257/E25.	.002	.All devices being of same type, e.g., assemblies of rectifier diodes (EPO)
			257/E25.	.022	
			257/E25.	.023	Device consisting of plurality of semiconductor or other solid-state devices
or	C	ompon	ents		
eα	rat	ted c	ircuit		formed in or on common substrate, e.g., int
09					device (EPO)
	3	324/	158.1	(0	OR, 3 XR)
		·	Class	324	: ELECTRICITY: MEASURING AND TESTING MISCELLANEOUS
	_	/			
	3	333/			OR, 0 XR) : WAVE TRANSMISSION LINES AND NETWORKS
					LONG LINE ELEMENTS AND COMPONENTS
			333/246		.Strip type
			333/247		Semiconductor mounts
	3	365/	200	(2	OR, 1 XR)
			Class	365	: STATIC INFORMATION STORAGE AND RETRIEVAL
					READ/WRITE CIRCUIT
			365/200		.Bad bit
	3	438/	15	(2	OR, 1 XR)
			Class	438	: SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS
			438/14		
			438/15		.Packaging (e.g., with mounting, encapsulating
′					etc.) or treatment of packaged semiconducto
r					
	3	714/	724	(1	OR, 2 XR)
	_				: ERROR DETECTION/CORRECTION AND FAULT
					DETECTION/RECOVERY
			714/699 714/724		PULSE OR DATA ERROR HANDLING .Digital logic testing
			114/124		.Digital logic testing
	2	257/	678		OR, 2 XR)
			Class 257/678		: ACTIVE SOLID-STATE DEVICES HOUSING OR PACKAGE
			231/010		HOOSING ON PACKAGE
	2	257/			OR, 2 XR)
			Class 257/688		: ACTIVE SOLID-STATE DEVICES .With large area flexible electrodes in press
			231/000		contact with opposite sides of active semi

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conductor chip
and surrounded by an insulating element, e
.g., ring 257/730 .Outside periphery of package having specified shape or configuration
2 257/777 (0 OR, 2 XR) Class 257: ACTIVE SOLID-STATE DEVICES 257/734 COMBINED WITH ELECTRICAL CONTACT OR LEAD 257/777 .Chip mounted on chip
2 257/778 (1 OR, 1 XR) Class 257: ACTIVE SOLID-STATE DEVICES 257/734 COMBINED WITH ELECTRICAL CONTACT OR LEAD 257/778 .Flip chip
2 257/E21.512 (0 OR, 2 XR) Class 257: ACTIVE SOLID-STATE DEVICES 257/E21.001 PROCESSES OR APPARATUS ADAPTED FOR MANUFACTURE
OR TREATMENT OF SEMICONDUCTOR OR SOL ID-STATE DEVICES OR OF
PARTS THEREOF (EPO)
257/E21.002 .Manufacture or treatment of semiconductor device (EPO)
257/E21.04Device having at least one potential-jump barrier or surface barrier, e.g., PN j
unction, depletion
layer, carrier concentration layer (EP
0)
257/E21.499Assembling semiconductor devices, e.g., packaging , including mounting, encapsu
lating, or
treatment
of packaged semiconductor (EPO)

257/E21.506

of packaged semiconductor (EPO)Attaching or detaching leads or other conductive members, to be used for carry

ing current to or

from device in operation (EPO)

257/E21.509Involving soldering or alloying process, e.g., soldering wires (EPO)

257/E21.511Mounting on insulating member provided with metallic leads, e.g., flip-chip mount

ing, conductive

die mounting (EPO)

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		09548826 CLSTITLES
2	257/E21.512	-
	23.004 (0	
		: ACTIVE SOLID-STATE DEVICES
2	25//E23.001	PACKAGING, INTERCONNECTS, AND MARKINGS FOR
S (EPO)		SEMICONDUCTOR OR OTHER SOLID-STATE DEVICE
· ·	257/E23.003	.Mountings, e.g., nondetachable insulating
_	207, 1123.003	substrates (EPO)
2	257/E23.004	
		, , , , , , , , , , , , , , , , , , ,
2 257/E2	23.069 (0	OR, 2 XR)
		: ACTIVE SOLID-STATE DEVICES
2	257/E23.001	PACKAGING, INTERCONNECTS, AND MARKINGS FOR
TORG (EDO)		SEMICONDUCTOR OR OTHER SOLID-STATE DEV
ICES (EPO)	257/E23.01	.Arrangements for conducting electric current
2	.57/ E25.01	to or from solid-state body in operatio
n, e.g., le	eads,	to of from botta beate body in operation
, , ,	,	terminal arrangements (EPO)
2	257/E23.023	Consisting of soldered or bonded
		constructions (EPO)
2	257/E23.06	Leads, i.e., metallizations or lead frames
: (EDO)		on insulating substrates, e.g., chip carr
iers (EPO)	257/E23.068	Additional leads joined to metallizations
2	.577E25.000	on insulating substrate, e.g., pins, bumps
, wires, fl	Lat	on insulating substitute, e.g., pins, bumps
•		leads (EPO)
2	257/E23.069	Spherical bumps on substrate for external
		connection, e.g., ball grid arrays (BGA) (E
PO)		
2 257/E2	22 07 /0	OR, 2 XR)
		: ACTIVE SOLID-STATE DEVICES
		PACKAGING, INTERCONNECTS, AND MARKINGS FOR
-	.0,7 220.001	SEMICONDUCTOR OR OTHER SOLID-STATE DEVI
CES (EPO)		
2	257/E23.01	.Arrangements for conducting electric current
		to or from solid-state body in operation
, e.g., lea	ads,	
) E7 / E22 A22	terminal arrangements (EPO)
2	257/E23.023	Consisting of soldered or bonded constructions (EPO)
2	257/E23.06	Leads, i.e., metallizations or lead frames
2	,	on insulating substrates, e.g., chip carri
ers (EPO)		The state of the s

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257/E23.07Geometry or layout (EPO)

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2		324	OR, 2 XR) : ELECTRICITY: MEASURING AND TESTING FAULT DETECTING IN ELECTRIC CIRCUITS AND OF ELECTRIC COMPONENTS .Of individual circuit component or element
	324/754		With probe elements
2	324/758 Class 324/500	324	: ELECTRICITY: MEASURING AND TESTING
	324/537 324/754 324/758		
2	333/33 Class 333/24R 333/32 333/33	333	: WAVE TRANSMISSION LINES AND NETWORKS
2	•		OR, 2 XR) : ELECTRICITY: ELECTRICAL SYSTEMS AND DEVICES
	361/600 361/679 361/683 361/684		HOUSING OR MOUNTING ASSEMBLIES WITH DIVERSE ELECTRICAL COMPONENTS .For electronic systems and devicesComputer related supportMemory unit support
2	361/783 Class		OR, 2 XR) : ELECTRICITY: ELECTRICAL SYSTEMS AND DEVICES
	361/600		HOUSING OR MOUNTING ASSEMBLIES WITH DIVERSE
	361/679 361/748 361/760 361/783		ELECTRICAL COMPONENTS .For electronic systems and devicesPrinted circuit boardConnection of components to boardHaving semiconductive device
2	365/230	365 .01	OR, 2 XR) : STATIC INFORMATION STORAGE AND RETRIEVAL ADDRESSING .Plural blocks or banks
2	713/2 Class		OR, 0 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING

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UP,	713/1	09548826_CLSTITLES SYSTEMS: SUPPORT DIGITAL DATA PROCESSING SYSTEM INITIALIZATION OR CONFIGURATION (E.G., INITIALIZING, SET
·	713/2	CONFIGURATION, OR RESETTING) .Loading initialization program (e.g., booting
,	222	rebooting, warm booting, remote booting, BI
05,	initial	<pre>program load (IPL), bootstrapping)</pre>
2	714/25 Class	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT
	714/100	DETECTION/RECOVERY DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
	714/1 714/25	.Reliability and availabilityFault locating (i.e., diagnosis or testing)
2	714/44 Class	OR, 1 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/100	DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
	714/1 714/25	<pre>.Reliability and availabilityFault locating (i.e., diagnosis or testing)</pre>
	714/40 714/44	Component dependent technique Peripheral device component fault
2	714/46 Class	
	714/100	DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
	714/1 714/25	<pre>.Reliability and availabilityFault locating (i.e., diagnosis or testing)</pre>
g	714/46	Operator interface for diagnosing or testin
2	714/47 Class	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/100	DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

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	714/1 714/47	Reliability and availabilityPerformance monitoring for fault avoidance
2	714/732 Class	(1 OR, 1 XR) 714 : ERROR DETECTION/CORRECTION AND FAULT
	714/699	DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING
	714/724	.Digital logic testing
	714/732	Signature analysis
2	714/733	(1 OR, 1 XR)
	Class	714: ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/699	PULSE OR DATA ERROR HANDLING
	714/724	.Digital logic testing
	714/733	Built-in testing circuit (BILBO)

09548826 LIST

PLUS Search Results for S/N 09548826, Searched February 20, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear ch

system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that a re

most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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4841434
5805606
5249450
5336649
5342807
5359547
5652754
5727000
5808919
5954827
6049896
6133745
6415397

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Most Frequently Occurring Classifications of Patents Returned From A Search of 09548826 on February 20, 2004

4 365/201 714/718 3 257/48 3 324/765 3 333/247 2 365/200 2 438/15 2 713/2 Cross-Reference Classifications 5 324/755 4 257/723 4 365/233 3 257/203 3 257/E21.525 3 257/E23.171 3 257/E25.023 3 324/158.1 3 324/765 3 714/718 2 257/678 2 257/730 2 257/777 2 257/E21.512 2 257/E23.004 2 257/E23.069 2 257/E23.07 2 324/754 2 324/758 2 333/33 2 361/684 2 361/783 2 365/201 2 365/230.03 2 714/25 2 714/47 714/724 Combined Classifications 7 714/718 6 324/755

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324/765 365/201

Original Classifications

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- 257/203 4
- 4 257/48
- 4 257/723
- 4 365/233
- 3 257/E21.525
- 3 257/E23.171
- 3 257/E25.023
- 3 324/158.1
- 3 333/247
- 3 365/200
- 3 438/15
- 3 714/724
- 2 257/678
- 2 257/730
- 2 257/777
- 257/778
- 2 257/E21.512
- 2 257/E23.004
- 2 257/E23.069
- 2 257/E23.07
- 2 324/754
- 2 324/758
- 2 333/33
- 2 361/684
- 2 361/783
- 2 365/230.03
- 713/2
- 2 714/25
- 2 714/44
- 2 714/46
- 2 714/47
- 2 714/732
- 714/733